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High Reliability Plastic Packaging for Microelectronics

James N. Sweet, David W. Peterson, Alex H. Hsia, Melanie Tuck

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

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James N. Sweet, David W. Peterson
Alex H. Hsia, Melanie Tuck
Advanced Packaging Department
Sandia National Laboratories
P.O. Box 5800
Albuquerque NM 87185-1082

Abstract

This Laboratory Directed Research & Development (LDRD) project conducted in fiscal years 1996 and 1997 under case 3526.030 was devoted to the development of test structures and associated measurement methodology for assessing the reliability of plastic encapsulated microelectronic devices. The end goal was the conceptual specification of one or more Assembly Test Chips (ATCs) which could be used evaluating plastic encapsulation technologies. In the course of this work we demonstated suitable circuits for measuring Au-Al wirebond and Al metal corrosion failure rates during accelerated temperature and humidity testing. We also showed that the test circuits on our ATC02.5 chip were very sensitive to extrinsic or processing induced failure rates. A number of accelerated aging experiments were conducted with unpassivated triple track Al structures on the ATC02.6 chip to demonstrate that these would be extremely sensitive to environmental conditions. We found an unexpected result, the unpassivated tracks were very sensitive to particulate contamination which caused conductor damage and resultant high voltage breakdown. A number of modifications to existing circuitry were suggested as a result of the unpassivated device experiments. We also showed that the piezoresistive stress sensing circuitry which we had designed for the ATC04 test chip was suitable for determining the change in the state of mechanical stress at the die when both initial and final measurements were made near room temperature. However, our attempt to measure thermal stress between room temperature and a typical polymer glass transition temperature failed because of excessive die resistor-substrate leakage currents at the high temperature end. Suitable circuitry changes were developed which should eliminate this problem. One temperature and humidity experiment was conducted with Sandia developed static random access memory (SRAM) parts to examine non-corrosion CMOS failures. This experiment did not achieve the desired objective because of processing problems but we did demonstrate that we could easily detect and measure a new type of corrosion failure mode, this time at the metal to Si contacts on the die surface. As a result of this two year effort, we have new designs for a number of test circuits which could be used on an advanced ATC for reliability assessment in Defense Programs electronics development projects.

Contents

I. Introduction

A. General Background

The LDRD project, *High-Reliability Plastic Packaging for Microelectronics*, was conducted during the FY95-FY96 (10/94-9/96) time frame. In the project proposal, two major objectives for the project were stated:

1. Determine and develop a fundamental understanding of packaging related failure mechanisms in commerical molded plastic ICs.

2. Use this as a basis for development of sensitive, state-of-the-art, active and passive test structures, testing methodology, and reliability models.

In this report we shall discuss to what extent the above objectives were achieved. In the area of passive test structures, we achieved significant success and demonstrated that our proposed test structures are capable of making quantitative measurements on factors directly related to the reliability of Plastic Encapsulated Microelectronics (PEMs). Our work with active test structures did not proceed as far as we had hoped because of difficulties in fabricating static random access memories (SRAMs) integrated circuits (ICs) in the Sandia Microelectronics Development Laboratory in time to do the planned experiments. Nevertheless, we did succeed in demonstrating that accelerated moisture testing of the SRAMs could detect a wafer fabrication related failure mechanism.

At this writing, the use of PEMs in Sandia developed Defense Programs (DP) weapons electronics systems is a subject of much current debate. The Department of Defense (DoD) has turned increasingly to the use of PEMs and Commercial Of the Shelf (COTs) components. Previously, DP electronics systems relied on Ceramic Hermetic Packaging (CHP) to protect ICs from environmental damage. However, the availability of ICs in CHP has decreased drastically since the last DP weapons electronic systems were designed and put into production. In addition, modern High Density Surface Mount (HDSM) Printed Circuit (PC) board technology relies almost exclusively on the use of plastic encapsulated ICs, as CHPs with the same footprint are generally not available.

In published comparisons of PEMs and CHP reliability, the observed failure rates are generally comparable or somewhat better for PEMs. However, these data are usually obtained from applications where the environment is relatively benign and this has been a basis of criticism in the past. Experience with PEMs in commercial avionics systems has been quite positive and most major manufacturers are relying exclusively on PEMs and HDSM. Much of the reliability associated with PEMs and HDSM is believed to be a result of automated mass production of both ICs and PC boards. The ICs are molded in large volume on completely automated assembly lines. The materials used in and the cleanliness of the unit operations are rigorously controlled to minimize the potential for package induced failure. Likewise, the mounting and soldering of parts

to PC boards is completely under machine control, although in this case volumes may be low or modest.

For DP electronics packaging and board assembly it may not always be possible to make use of the advantages associated with mass production. A weapons electronics system will probably use at least a few custom or special ICs which have to be packaged in low volume, possibly by a contract assembly facility. In such a case, it would be highly desirable to have a means of evaluating the quality of the assembly process from a reliability viewpoint.

B. Failure Modes in PEMs

In the past, the main concern with the use of PEMs for high reliability DoD and DOE applications has been the lack of hermeticity associated with plastic packages. All polymers are permeable to moisture and hence some water will inevitably be present at the surface of the IC. However, this moisture does not automatically result in damage to the IC. Other constituents such as ionic contamination and high temperature must be present to enable known failure modes. In modern IC parts, ionic contamination is reduced to extremely low levels in both the wafer fabrication and plastic molding operations. As a result, corrosion of conductors in commercial ICs is extremely rare. However, it is possible to cause circuit damage and even failure by using very high temperatures, humidities, and bias voltages in an accelerated Temperature Humidity Bias (THB) test. A pressurized THB test run at a temperature above the boiling point of water is referred to as a Highly Accelerated Stress Test or HAST. On common commercial parts, a HAST at 160°C and 85% relative humidity (RH) will produce measurable failures in 100's of test hours.

Unlike common tests for CHP such as leak rate measurements, a THB test on plastic parts in generally considered to be destructive, especially if measurable failures are observed. Hence THB tests cannot be used to "screen" PEMs although, as we shall discuss, they are very useful as both a sampling test and a method to evaluate materials and processes. Manufacturers of high reliability avionics systems frequently run THB tests on samples from vendor parts to insure that adequate moisture resistance is achieved in their product.

Although early in the history of PEMs (1968-1980), the major concern in high temperature and humidity environments was corrosion of Al metal on the IC, in more recent times attention has shifted to moisture induced damage to metal-oxide-semiconductor (MOS) transistor structures. There have been reports of moisture induced failures in MOS transistors associated with threshold voltage shifts presumably caused by moisture penetration into the transistor gate oxide structure. On of the goals of this LDRD work was to look at the use of CMOS SRAM test circuits for examining this moisture related failure mechanism.

The focus of concern in commercial manufacturing has shifted to issues associated with sudden moisture release during high temperature solder reflow during mounting of the ICs to the PC board. This so called "popcorn" effect can cause cracking in the package or delamination of interfaces inside the package. Although cracking and delamination do not usually produce a functional failure of the device, they are potential long term reliability issues. In the case of custom assembly of DP systems, it is possible to vacuum bake the PEMs prior to surface mount in

order to drive any moisture out of the package, thus minimizing the possibility of popcorn damage.

Another concern in commercial IC packaging is the occurrence of high mechanical stress at the IC surface as a result of differential thermal contraction of mold compound and IC die as the part cools from the molding and curing temperatures to ambient. Excess stress can produce cracking or damage to metal conductors on the IC surface. In addition, some circuits such as analog are susceptible to stress induced shifts in certain circuit parameters. The measurement and control of packaging related stresses is a major issue in some areas of packaging.

An emerging concern for parts subjected to high temperatures is the stability of the Au wire bonds to the Al bond pads on the IC. At sufficiently elevated temperatures, brittle intermetallics can form, resulting in a loss of bond strength and possibly an electrical open circuit. Since the mold compound holds the wires in a state of compression with the IC, it is possible or even likely that bonds with extremely low strength will be maintained in an electrically conducting state. Hence, function testing cannot usually find this type of "latent" failure. At temperatures $\geq 150°C$ this type of failure becomes possible. The failure rate has been found to be enhanced by the presence of bromine flame retarding materials in the mold compound. The failure rate is enhanced by the presence of moisture.

We can summarize this section by listing the known or possible failure mechanisms of PEMs in hostile environments:

1. Temperature and moisture induced corrosion of Al conductors and bond pads on the IC.

2. Temperature and moisture induced weakening and damage to Au-Al wire bonds on the IC.

3. Temperature and moisture induced damage to transistor structures in the IC.

4. Damage to the packaged IC during surface mount solder reflow caused by sudden moisture release (popcorn effect).

5. Mechanical stress induced die cracking or damage to metal conductors on the IC from shear stresses.

C. Use of Test Chips

We have developed a number of special purpose Assembly Test Chips (ATCs) to study environmentally produced damage and failure in plastic encapsulated ICs. The work described here extends our preliminary investigations and leads to a conceptual design of several potential new ATCs which could be used in DP electronics programs for either process development or qualification of a small volume custom assembly facility. However, some residual questions still exist which were not answered in the research described below.

II. Passive Test Structures

A. Wire bond degradation test structure

One of the major goals of this project was the development and proof testing of a structure which could be used to measure bond degradation with only an electrical measurement. Traditionally, this failure mode is observed by first removing the plastic from above the encapsulated IC die and then measuring the force required to either pull or shear the bond wires from the die. This is, by definition, a destructive test, and one which is both expensive and laborious to conduct.

A full description of the development of our bond resistance test structure and its use in actual experiments has been given in a recent report on the fiscal year (FY) '96 work on the DP sponsored Microelectronics Plastic Molded Packaging (PMP) program[1]. Here we give a brief description of the development of the test structure which we used for the PMP experiments.

A drawing of an Au wire bond to an Al pad on an IC is shown in Fig. 1.

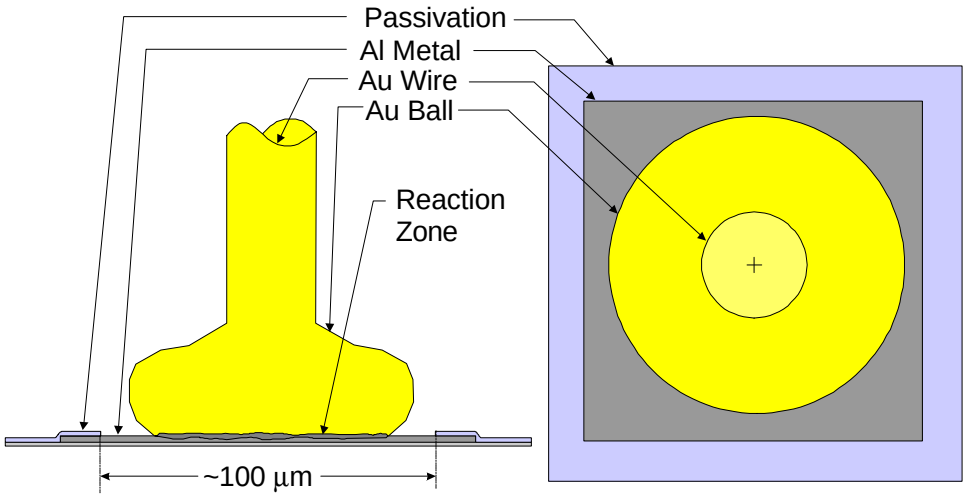


Fig. 1 Au bond on an Al bond pad showing a conceptual picture of a reaction zone under the bond. (a) Side view showing the "ball", approximately 75 µm in diameter. (b) Top view. The Al metal under the Au ball is about 1.5 µm thick. Most of the reaction zone is located in the Al region.

Ideally, it would be desirable to measure the resistance of just the reaction zone shown in Fig. 1. However, in an actual measurement there is extraneous series resistance from the wire and the pad which makes it difficult to determine the change in resistance due to reaction zone formation. This change may be only a few mΩ, while the series resistance is in the range ≈ 100-500 mΩ. A method of making an approximate measurement was described by Blish and Parbek[2]. They used a chip with a sheet of Al metal and connections which required multiple bonds to leadframe contact fingers. They determined that a resistance change ~ 20 mΩ corresponded to significant losses of both pull and shear strength. Although their design appears to have worked well, we desired to

have a test structure which could be conventionally bonded so that wire bond assembly could be performed just as it is in actual practice, with one wire per leadframe finger.

Instead of measuring the resistance to current flow through the bond under study, as shown in Fig. 1, we decided to test the hypothesis that the resistance to current flow through the bond and its included reaction zone would show the same type of resistance increase that a true bond resistance measurement would. Such a circuit is shown conceptually in Fig. 2. Initially, after bonding, current shunts through the Au ball, resulting in a resistance decrease. After reaction zone formation, the resistance would be expected to increase if this zone is in the Al region.

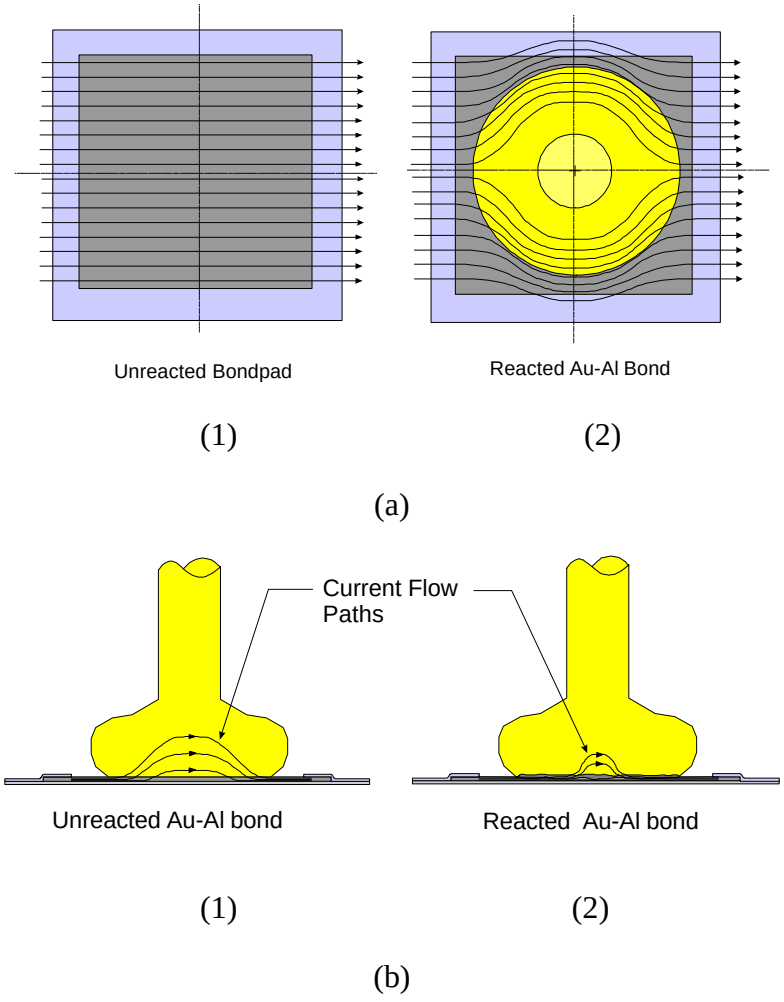


Fig. 2 Conceptual transverse bond resistance structure. (a) Top view. (b) side view. Prior to bonding, the current flows uniformly through the Al bondpad sheet, (a1) . After bonding, some of the current is shunted through the Au ball, resulting in a lowering of the transverse resistance, (b1). After formation of a highly resistive interfacial reaction zone, the current tends to flow around the ball (a2) and the current shunting through the Au ball is decreased (b2). As a result, the resistance to transverse current flow increases.

An actual SEM micrograph of a Au ball bond is shown in Fig. 3.

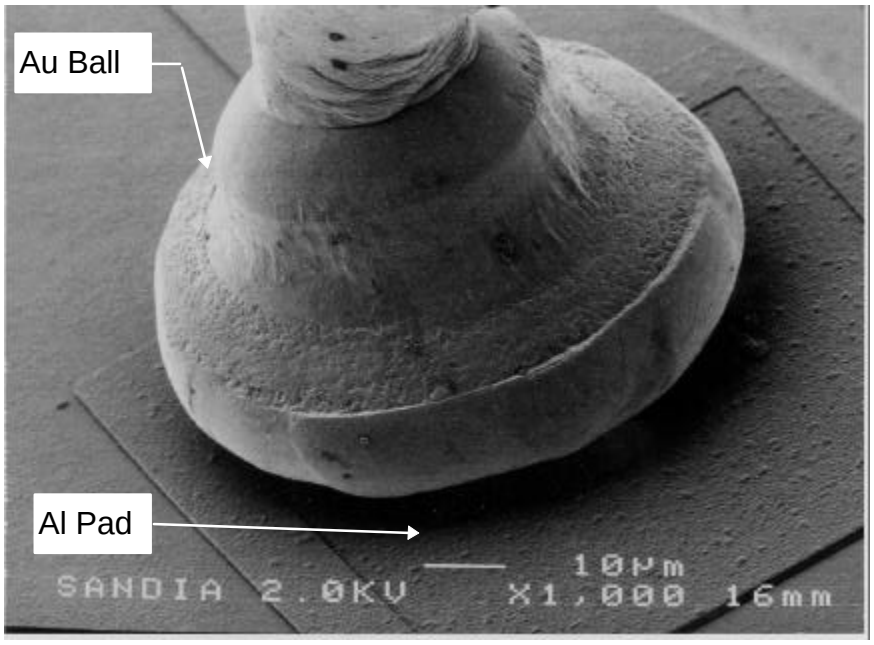


Fig. 3 SEM micrograph of an Au ball bond on an Al bondpad. The bond in this photo is somewhat off center.

In order to test the concept we used a circuit on the ATC03 chip which was originally intended to be used for measurement of bond pad placement[3]. A schematic diagram of this structure is shown in Fig. 4.

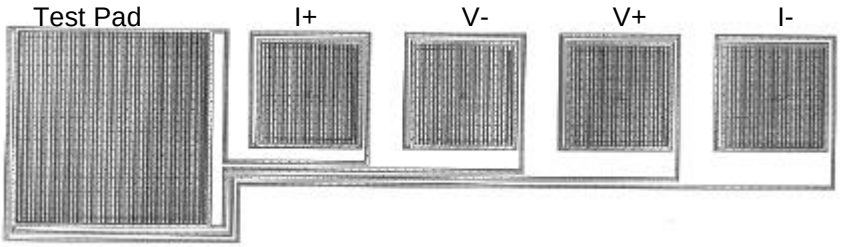


Fig. 4 ATC03 bond pad placement structure. For the transverse resistance measurement, the current and voltage high are I+ and V+, respectively and the current and voltage low are I- and V-.

The corners of the large pad are each connected to the four small pads on the right. This enables a measurement of the resistance across the diagonals of the large bond. We used a four terminal measurement geometry with the current lines being on one side of the large pad and the voltage measurement lines on the other side.

We measured the transverse resistance before and after wire bonding and then at a number of times during a 300°C low humidity aging test. The reactions under study are known to proceed very rapidly at this temperature, even with no encapsulation material present. A graph of the

measured resistance for an average of eight bonded and two unbonded or control pads is shown in Fig. 5.

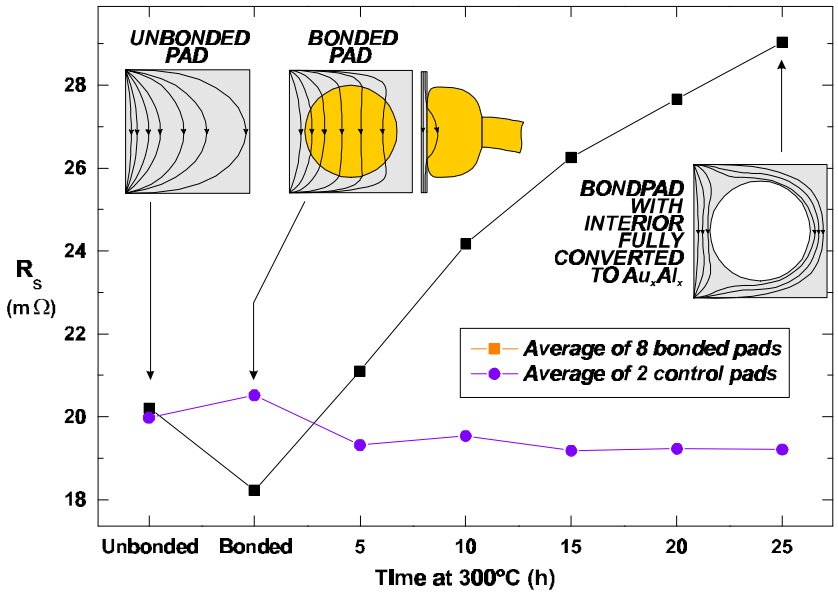


Fig. 5 Change in ATC03 bond pad position sheet resistance as a function of aging time at 300°C.

The initial drop in resistance due to ball shunting is clearly evident, as is the increase in tranverse resistance with time at 300°C. A scanning electron micrograph of the structure after 30 h at 300°C is shown in Fig. 6.

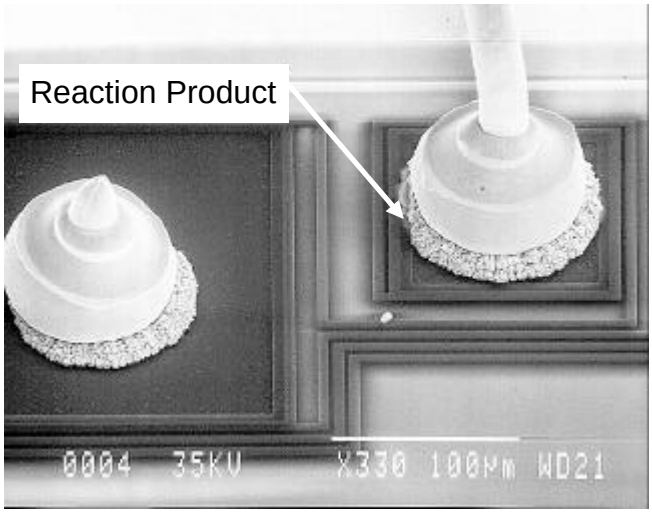


Fig. 6 ATC3.0 bond pad position test structure showing intermetallic growth after 30 hours at 300 °C.

The Au/Al intermetallic reaction zone is clearly evident around and under the Au balls in Fig. 6. The net change in resistance was only about 10 mΩ, but this was from an initial value of 18 mΩ,

so the resolution of the measurement was excellent. Since the bond pad we used was larger than a normal pad, the measured resistance change was smaller than we would expect to see from a normal pad. The success in this experiment led us to design a new structure for the ATC02.6 Assembly Test Chip.

The ATC02.6 chip has 22 bond pad resistance structures of the type shown in Fig. 7

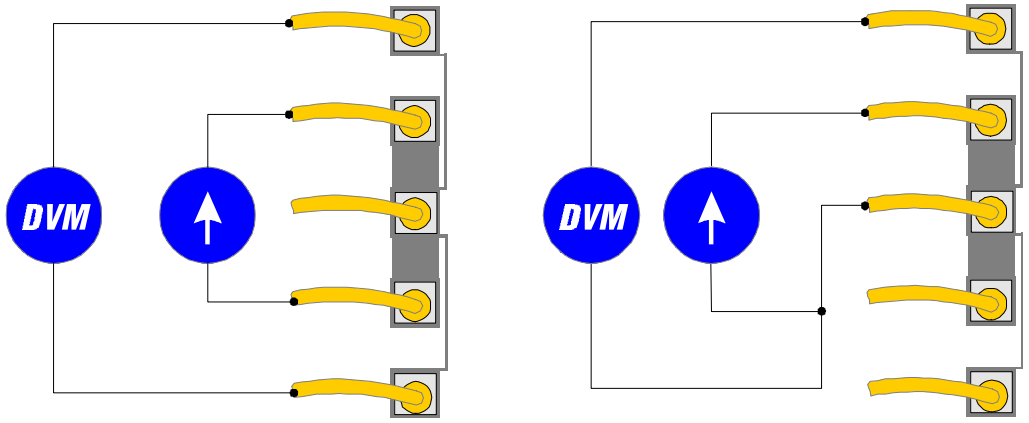


Fig. 7. One of 22 bond pad resistance structures showing typical measurement connection for 4-point interfacial resistance of the center bond wire/bond pad (left) and 3-point measurement of the center bond wire continuity (right).

Current is supplied uniformly to the bond under test (BUT) through two adjacent pads. The next two outer pads are used to measure the voltage drop across the BUT. We also measured the bond resistance directly with the three terminal connection shown on the right. This connection includes the resistance in the wire connected to the BUT as well as the package lead resistance for that wire, since the DVM and current source are connected external to the package. In practice, this extraneous resistance introduced enough variability so as to make the measurement of limited utility.

Detailed results on experimental high temperature tests with CHP control parts and with three different epoxy molding compounds are given in Ref. 1. A typical result from a 200°C test is shown in Fig. 8 for molded plastic packages with a mold compound in high use today. Also shown are the results of bond pull and shear tests on samples removed from the test at succeeding measurement points. At the initial measurement time the average pull and shear strengths show an increase, indicating the initial reaction actually results in strengthening the bond. As time progresses, both average shear and bond pull strengths show a marked decrease, while the resistance increases to a plateau.

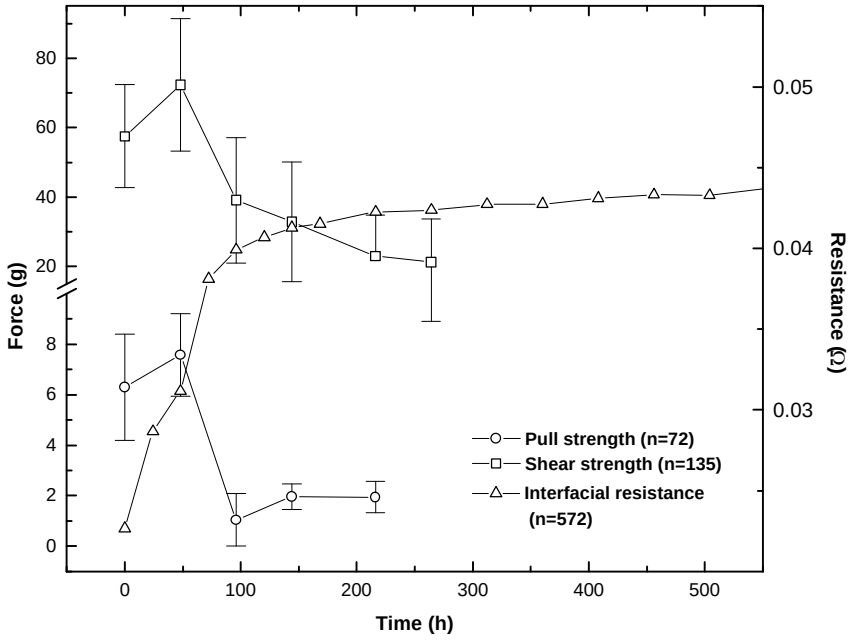


Fig. 8. Plot of ATC2.6 average interfacial bond resistance (triangle, right ordinate) as a function of time at 200°C of 572 test structures assembled in 160 lead PQFP packages using Sumitomo 6300HJ epoxy novolac baseline molding compound. First 500 h of 1152 h experiment are shown. Overlaid are average bond shear strength (square) and pull strength (circle) data in grams on left ordinate vs. time. Error bars represent one sigma standard deviation.

The results of these experiments indicate that the simple structure we have developed works well for making noninvasive electrical measurements of Au-Al bond degradation during high temperature storage experiments. The measurement is very sensitive and standard deviations associated with it are very small. As a result it is possible to derive accurate bond degradation rates with a small sample size, In contrast, the standard deviations associated with bond pull and bond shear measurements are quite large, necessitating the use of large sample sizes.

B. Corrosion test structures

1. Design considerations

Corrosion testing is commonly performed with interdigitated conductor structures called triple tracks. These consist of three parallel serpentine tracks, with the outer tracks commonly biased positively and the inner track negative. The very high electric fields which exist between adjacent conductors in the track structure can result in rapid electrochemical corrosion of Al conductors in the presence of moisture and mobile ions. Such ions can be present either in contaminants on the die surface or in the mold compound. Although the conductors have a protective passivation layer, typically SiN, an pinhole or defect in this passivation can result in corrosion starting at the defect site. This corrosion will proceed rapidly at high bias, resulting in an open circuit of one or

more tracks in a structure. It is evident that the track structure not only measures the intrinsic degradation rate associated with corrosion produced by background ionics but also the extrinsic degradation rate associated with passivation defects. As a result, triple track testing has a wider applicability than just measurement of corrosion rates.

In addition to corrosion of the conductors in the track structure, corrosion can occur on bond pads. In defect free passivation layers, this is the most common failure mode observed. Corrosion rate tests are commonly performed in a HAST system at temperatures of 140°C or above and at 85% relative humidity. In addition, the bias voltage is usually set higher than the nominal value, 5 V.

In experiments conducted with our ATC01 corrosion test chip prior to the start of this LDRD we observed that there was a high degree of statistical variability in this type of testing. As a result, we decided to include as many triple tracks as possible in the test die developed for this project. However, each triple track required six bond pads for electrical connection, so it would be difficult to put a large number of separate tracks on a die. As a result of this consideration, we decided to experiment by connecting one end of each track to a common bus, resulting in a near halving of the required number of die connections required. A schematic diagram of the structure which we have tested on the ATC02.5 and ATC02.6 parts is shown in Fig. 9. In both of these parts the triple tracks were designed with 2 μm line with and line to line gap dimensions, typical of the top level of Al metal in most IC technologies. The ATC02.5 die has twelve triple tracks and the ATC02.6 eight.

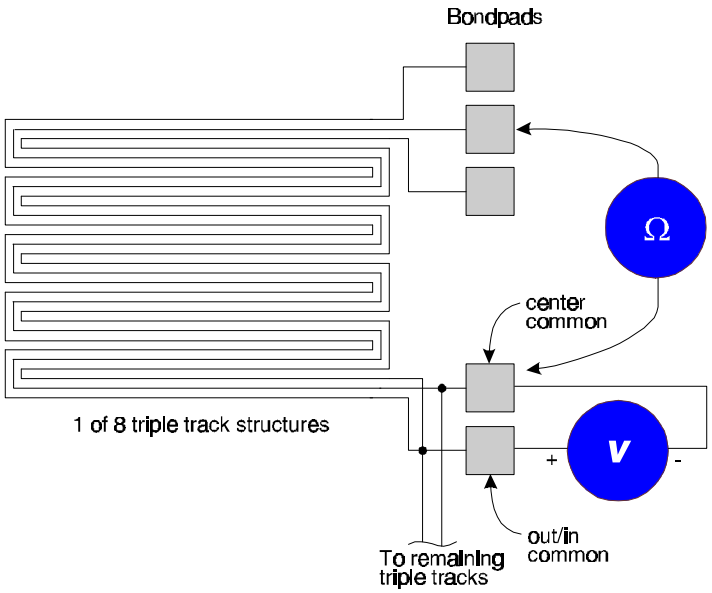


Fig. 9 Schematic diagram of triple track structure consisting of three interdigitated tracks, with the outer tracks typically biased anodically with respect to the center (cathodic) track. Track corrosion is detected by measurement of the track resistances, normally with the bias removed.

Another experiment which we attempted was the use of triple tracks with unpassivated regions. The ATC02.6 die was designed with eight triple tracks. Four of these triple tracks had square cutout windows in the passivation, thus exposing the tracks in the windows to the ambient environment. An SEM micrograph of one of these window regions is shown in Fig. 10.

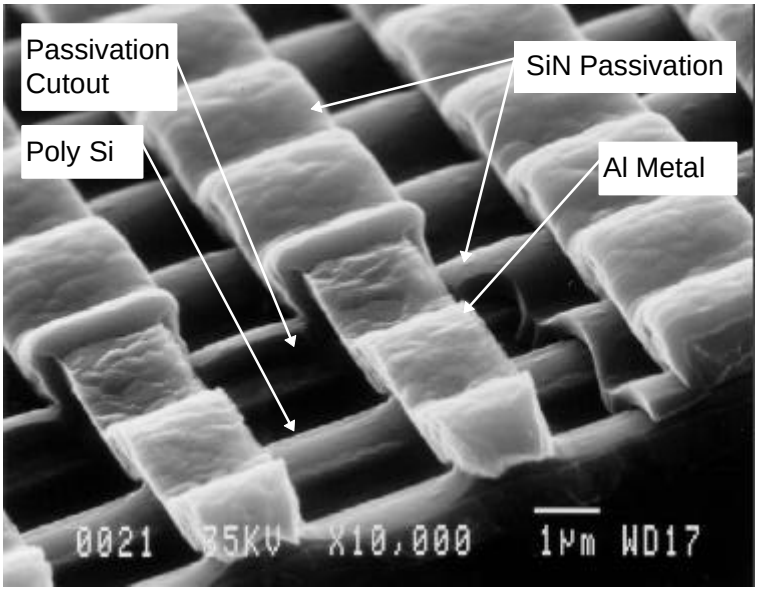


Fig. 10. ATC02.6 triple track structure showing a passivation cutout region. This design was intended to enhance the rate of corrosion failure.

We hoped that this design would enhance the corrosion induced failure rate because ions from the mold compound or surface contamination could easily reach the surface of the Al conductors and initiate corrosion there.

2. Test samples

We ran experiments with two types of test package samples. The first was a molded 160 lead plastic quad flatpack (PQFP) assembled by the IPAC Corp. The wafers were first lapped at the National Semiconductor Corp. to a final thickness of approximately 0.017 in. and then sent to IPAC for assembly. At IPAC, the wafers were diced and all assembly operations were performed with automatic equipment. The second type of package was made at Sandia and used liquid epoxy encapsulated samples. In this case, the unlapped die were attached and wire bonded in 40 lead CHP dual in-line packages (DIPs) and the cavity was then filled with a low viscosity liquid encapsulant in the Process Development Laboratory by Dept. 1472.

3. High voltage breakdown

Prior to running HAST experiments, we apply a 100 V voltage stress to the test parts in order to detect any possible defective die. Many of the PQFP ATC02.6 parts failed this test and after breakdown had shorted tracks. This was a serious problem with our design because any short would cause a short of all tracks as a result of the common bus structure. This problem was occasionally seen with ATC02.5 parts but at a much reduced level. Detailed failure analysis

measurements were made by Dept. 1275 and are described in detail in Ref. 1. Many of the observed failures were traced to mechanical damage of the conductors in the unpassivated window regions. This damage was presumably caused by particles which were driven into the surface during the molding operation. One possible source of particles is from wafer lapping or back grinding. In this process, a plastic adhesive tape is applied to the wafer front surface and the wafer is then mounted on a chuck for grinding. Another potential source was identified as existing contamination on the wafers prior to shipment to National Semiconductor for backgrinding. A third possible source was particulates from the mold compound. Typically, mold compounds are loaded with fused silica particulate filler to lower the coefficient of thermal expansion. During molding the mold compound is injected into the mold cavity under some pressure.

To test the general particulate contamination hypothesis, we probed die at the wafer level. In this case, few breakdowns were observed, indicating that loose particulate contamination from the ambient environment was not sufficient to initiate failure. It appears that encapsulation is required to activate the failure mode which we observed.

We established new procedures for achieving and maintaining wafer cleanliness during the assembly operation. Wafers were taken from storage and cleaned prior to shipment. During the backgrinding and subsequent assembly process, care was taken at every step to insure wafer cleanliness. These steps resulted in a much decreased failure rate, but this rate was not reduced to an insignificant level. It appears from this experiment that the unpassivated triple track regions are extraordinarily sensitive to particle induced damage.

In order to examine the hypothesis that the transfer molding process drove particles into the die surface, we made some samples at Sandia with liquid epoxy encapsulant, as described above. We were surprised to find that these parts were susceptible to high voltage breakdown also, even though the encapsulant was applied in the form of a low viscosity liquid at ambient pressure.

In summary, we found that ATC02.6 die with unpassivated triple track structures were highly prone to high voltage breakdown and that this process usually lead to a permanent low resistance short between the center tracks and either the outer or inner track buses. This failure rate could be reduced by careful cleaning and handling but we could not achieve a sufficiently low failure level so that we could use the ATC02.6 parts for THB accelerated aging experiments. The passivated ATC02.5 die also showed this same high voltage breakdown failure mode, but at a much reduced level. In this case we were able to screen parts and select those which did not breakdown for subsequent experiments. However, as we shall see in the next section, particulate damaged parts show an enhanced failure rate in HAST THB aging experiments.

4. HAST experiments

In order to test the use of our proposed triple track structure in a realistic THB experiment, we used parts similar to those being used in a reimbursible program, the DARPA sponsored Low Cost Packaging Technology Reinvestment Program. The 160L PQFP parts are typical of those widely used in current commercial (and military) surface mount PC board fabrication. The experiment which we conducted is described in detail in the PMP FY97 report, Ref. 1. Here we add some amplifying comments relative to the LDRD supported test structures development.

The parts were packaged with standard materials in high use today. A HAST experiment was conducted with a temperature of 140°C and 85% relative humidity. Parts were mounted in spring loaded sockets at bias voltages of 10 and 40 V. Another group of parts was placed on a tray in an unbiased state. Periodically, the HAST system was shutdown and the parts removed for electrical measurement.

The results of our first experiment are shown in Fig. 11.

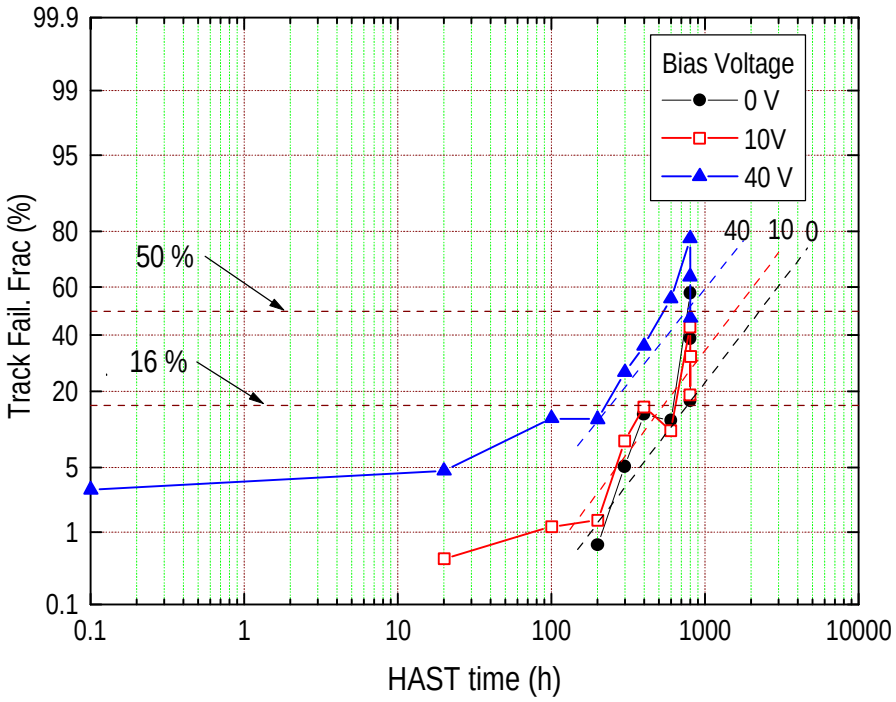


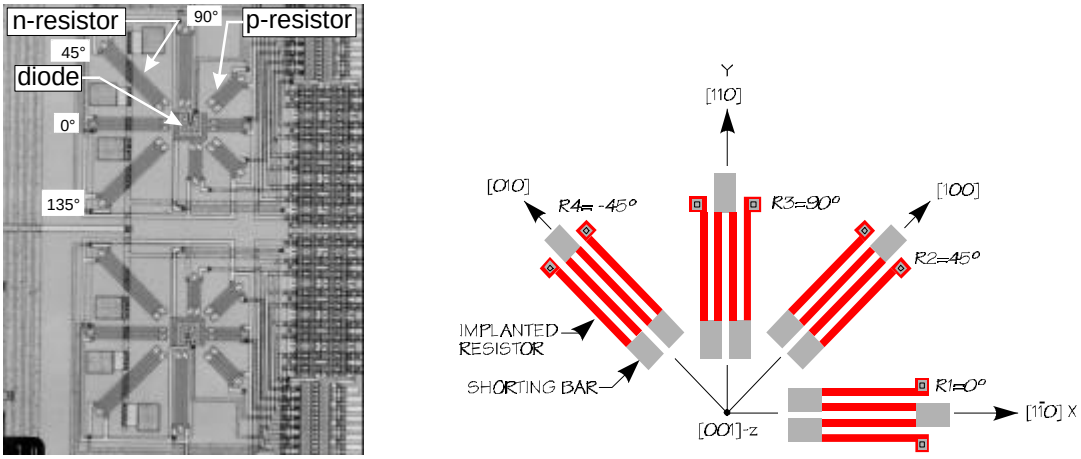
Fig. 11 Experimental cumulative distribution function for the 140°C 85% RH HAST. The 16 and 50% failure fractions are shown by the horizontal dashed lines. The data for each voltage group are extrapolated to higher failure fractions using the diagonal dashed lines. This extrapolation has been made “by eye”.

The parts for this experiment were assembled prior to instituting rigorous cleaning and particulate contamination control procedures. A second group of parts was fabricated with these new procedures and a small number was subjected to a new HAST. In this experiment we used six parts at each of six test conditions: two temperatures; 140 and 159°C and three bias voltages; 0, 10, and 40 V. After 1200 h the 140°C groups biased at 0 and 10 V exhibited very small cumulative failures, < 2% for each group. This can be contrasted with the results of the first experiment, Fig. 11, which shows a failure fraction of about 20% for both groups. This is another example of the improvement in part lifetime which can be achieved with good contamination and particle control procedures.

The two HAST experiments which we conducted served to validate the basic design of the ATC02.5 triple tracks shown schematically in Fig. 9. The use of common buses for the center track and inner/outer tracks results in a significant reduction in bond pad count without causing any trouble in collecting data. However, from the experience with the unpassivated ATC02.6 tracks, we found that it would be better practice to keep unpassivated structures electrically isolated from passivated structures so that the latter are not shorted if particulate damage occurs to the former.

III. Stress Measurement

At the time this LDRD research was started we had a stress sensor design implemented on the ATC04 Assembly Test Chip. This CMOS chip contains an array of 25 individually addressable stress sensing cells, each approximately 200 μm on a side, with a diode thermometer in the center of each cell. A cell contains four n-type and four p-type piezoresistors for stress measurement, as shown in Fig. 12.



(a) (b)

Fig. 12. ATC04 stress sensor cell. (a) SEM micrograph of two sensor cells showing the resistor layout and some of the addressing circuitry. At the center of each resistor "rosette" structure there is a diode used for cell thermometry. (b) Resistor layout used for analysis. The resistors numbered 1-4 correspond to 0, 45, 90, and 135°, respectively.

The use of the ATC04 chip in measuring mechanical stress in an encapsulated parts has been discussed by Sweet, Peterson, Emerson, and Burchett[4]. In this paper the basic functionality of the stress sensor cell was demonstrated and detailed measurements were made of the stress distribution over the die surface. As discussed, the stress is measured between some inital state and a final state. Frequently the initial state is taken as the bare die at the *wafer level* and the final state is taken as post-assembly. The wafer level electrical measurements are made with a probe system and the package measurements on a part inserted into a test socket. In general, any change in temperature between the initial and final state produces changes in the resistor values which are not caused by stress shifts and hence a correction for this temperature shift is required. Two stress tensor component linear combinations, σ_{xy} and σ_{xx}-σ_{yy} can be measured, in theory, without requiring a temperature correction because they are derived from the difference in resistance shifts of resistors with an identical geometry, differing only in orientation on the chip surface. In this discussion, we consider a coordinated system with the chip surface being the x-y plane and the z axis normal to the chip.

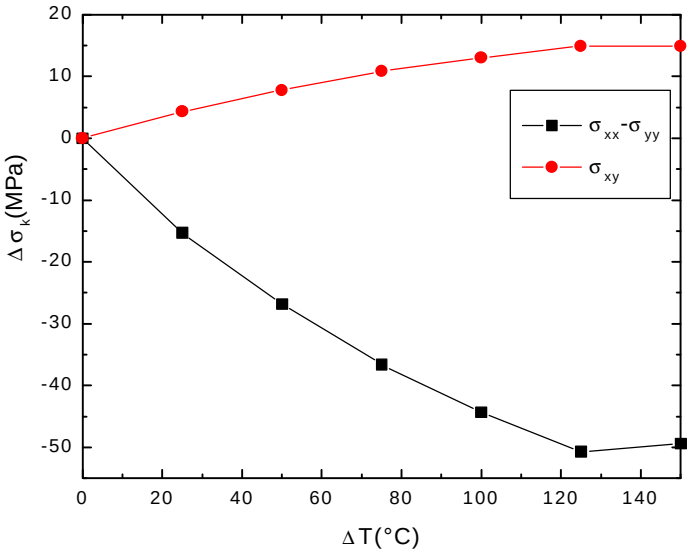
The in-plane compressive stress σ_{xx} can be measured approximately, but requires a temperature correction proportional to $\alpha\Delta T$, where α = temperature coefficient of resistivity and ΔT is the temperature change between the initial and final measurements. This is not too much of a problem

when measurements are made in a laboratory ambient environment with only a few °C temperature change. However, when measuring thermal stresses directly, it is desirable to heat the part up to mold compound glass transition temperature giving $\Delta T \sim 150°C$ or so. In addition to being able to make the temperature correction accurately, it is important to show that there are no current leakage paths at high temperature which could cause an error in resistance measurement.

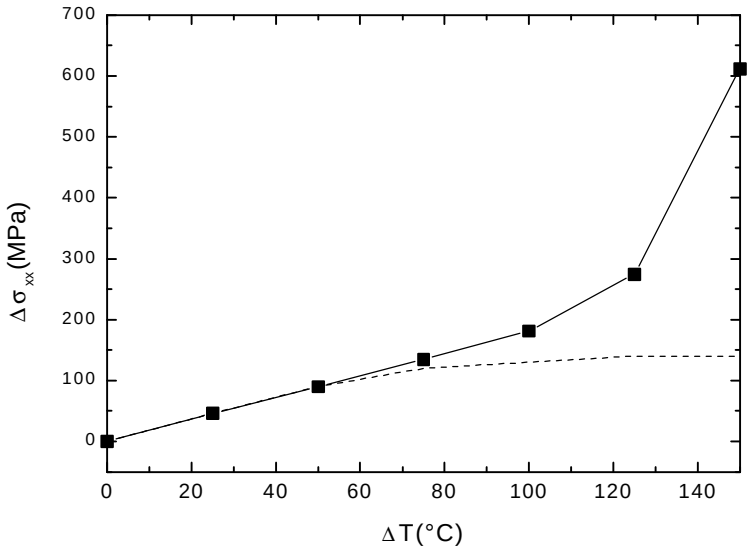
In an initial measurement we used a liquid encapsulated DIP with a single ATC04 die. The part was placed in an oven and the temperature was taken from room temperature to about 175°C. The diode measured temperature agreed well with the oven temperature as measured by thermocouple. At each temperature hold point the stress tensor components were measured with reference to the ambient, $T_0 \approx 25°C$. The measured stress component shifts or changes as a function of $\Delta T = T - T_0$ are shown in Fig. 13.

The shearing stress change is shown in Fig. 13(a) for a corner cell, a location where the amplitude of σ_{xy} is a maximum. The stress difference σ_{xx}-σ_{yy} is shown in Fig. 13(a) for a cell near the midpoint of a die edge where it has a maximum amplitude and the compressive stress σ_{xx} is shown for a cell in the die center in Fig. 13(b). Both of the measured quantities in Fig. 13(a) are intrinsically temperature compensated in that they are derived from the difference in resistance changes between two nominally matched resistors. Hence, any temperature induced shift in one resistor value is presumably matched by the same shift in the other resistor, leaving only stress induced shifts to produce a difference in the $\Delta R/R$ values for the two resistors used to calculate the stress component [4]. From the data in Fig. 13(a) it can be seen that both $\Delta\sigma_{xy}$ and $\Delta(\sigma_{xx}$-$\sigma_{yy})$ achieve a constant magnitude at $\Delta T \approx 125°C$. This corresponds to a temperature $T \approx 150°C$ which is near the glass transition temperature, T_g, for the encapsulant. At T_g the encapsulant enters a rubbery state and presumably communicates little or not stress to the die. Further heating to 175°C produces little stress, presumably because the epoxy die attach is also in a rubbery state.

In contrast to this behavior, The uncompensated σ_{xx} in Fig. 13(b) continues to increase and at a more rapid rate as the temperature becomes higher. The dashed line in Fig. 13(b) shows the expected variation in σ_{xx}. These σ_{xx} data suggest that the temperature compensation is not working correctly. Examination of the primary resistance data shows that the resistance values actually start to decrease with temperature at the higher ΔT values, indicating that there is a source of extra resistance in parallel with the resistor under test(RUT). This parallel resistance appears to decrease with increasing temperature, with the result that the resistance of the RUT eventually becomes dominated by the extraneous resistance.



(a)



(b)

Fig. 13. Measured stress changes from the ATC04 thermal stress measurement experiment. (a) Shearing stress, $\Delta\sigma_k=\sigma_{xy}$ and compressive stress difference, $\Delta\sigma_k=\sigma_{xx}-\sigma_{yy}$, functions. These measured quantities are temperature compensated and do not require an explicit temperature correction. (b) $\Delta\sigma_{xx}$ for the same part. The solid line and points are the measured data. The dashed line represents the expected variation of $\Delta\sigma_{xx}$ vs. Temperature.

Examination of the actual layout of the ATC04 chip suggested that the potential source of error was the reverse biased p-n junction leakage currents between the resistor and the well of opposite

doping type in which it was placed. Although this current is negligible near room temperature, it becomes appreciable at high temperature. All of the resistors on the chip were tied together at one end to facilitate ease in measurement. The other end of a resistor was isolated by CMOS transmission gate circuitry. Thus, the leakage current from all the wells could affect a measurement at high temperature.

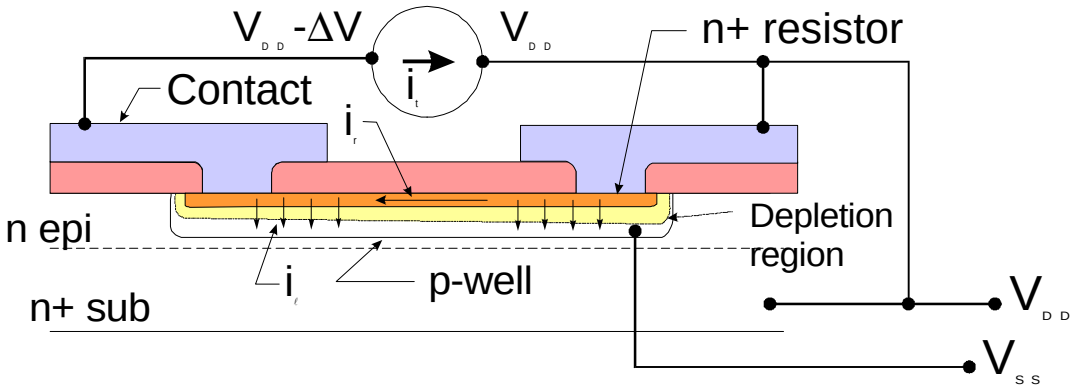


Fig. 14 Schematic cross-section of an implanted n-type resistor. The n+ implant is made into a lightly doped p-type well which is biased at the lowest potential, V_{SS}. The resistor is biased by a current source with its positive terminal connected to the power supply voltage, V_{DD}. The p-well and n+ resistor represents a reverse biased p-n junction diode. At high temperatures, a reverse bias leakage current flows between the resistor and the well.

A schematic diagram of an implanted n-type resistor is shown in Fig. 14. The implanted resistor is biased by a current source, connected as shown. The source supplies a current i_t to the contacts of the implanted resistor. An current i_r flows through the resistor producing a voltage drop $\Delta V=i_rR$, where R=resistance of the implanted resistor. The bias supply voltage is V_{DD} and the lowest or ground voltage is V_{SS}. The magnitude of ΔV must satisfy the relation, $V_{SS} \leq|\Delta V| \leq V_{DD}$ in order that the resistor to well junction not be forward biased anywhere along its length. In normal operation, the n+ resistor to p-well junction diode is reverse biased along its whole length. There is a small reverse bias leakage current, i_ℓ, which flows across the resistor to p-well junction, but at normal temperatures this is negligible relative to i_r. At elevated temperatures, i_ℓ increases rapidly in magnitude and if there is sufficient junction area, this magnitude can become on the order of $|i_r|$.

The ATC04 wafer has a number of QUality Enhancement STructures or QUEST which are used for process monitoring and various test functions. One of these structures is a test piezoresistance cell in which the resistors and associated well bias connections can be directly bonded, facilitating the measurement of leakage currents for a single resistor. The results of such a measurement for a p-type implanted resistor are shown in Fig. 15 as a function of temperature with the reverse bias voltage VR as a parameter.

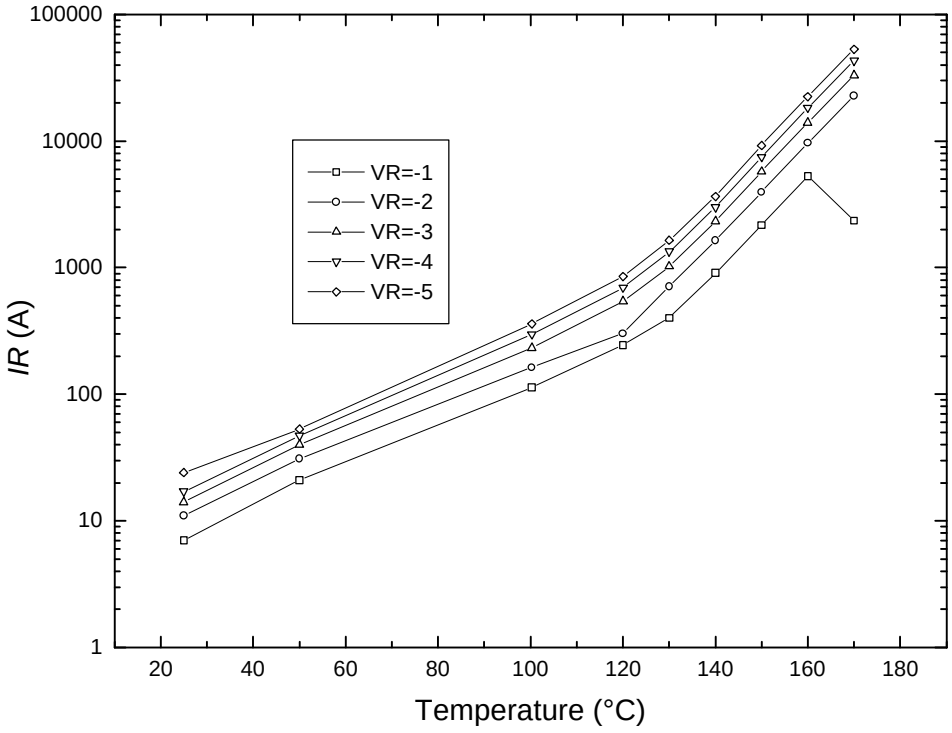


Fig. 15. Measured reverse bias leakage current from single *p*-type piezoresistor in a QUEST cell as a function of temperature with reverse bias voltage VR as a parameter. In normal operation, VR= -5 V.

The data from Fig. 15, along with similar measurement data for the *n*-type piezoresistor were used to develop model parameters for the SPICE circuit modeling program[5,6]. An Excel spreadsheet was used to develop model parameters that brought the simulation into convergence with the measured values of the p and n-type diodes over the temperature range using a multivariable variation method.

A detailed SPICE circuit simulation model was then developed to test the leakage current hypothesis. This model simulated the combined effects of 50 *p*-type and 50 *n*-type reversed biased junctions in a single ATC4.0 test chip during stress measurement. The distributed leakage currents shown in Fig. 14 were simulated by five diodes for each resistor. Using the derived SPICE parameters for these diodes, we verified in a semiquantitative way that the leakage current model could account for the observed variation of implanted resistor value vs. temperature. From this result, we determined that one resistor with its associated well leakage current would work well over the temperature range of interest and that the relatively simple design change of adding a transmission gate to the common side of each resistor would serve to isolate the RUT from other resistors on the chip. Although there is still leakage to the well of the RUT at high temperature, the resistor-well surface area for one resistor is not large enough to cause a measurement error, at least in the temperature regime in which we are interested.

IV. Active Test Structure SRAM

One of the most commonly used digital ICs for process development and evaluation of environmental stress sensitivity is the Static Random Access Memory or SRAM. This device is densely populated with MOS transistors and failure of any transistor on the IC will lead to at least the failure of one bit storage location in the memory[7]. This location can be precisely determined in a function test thus facilitating failure analysis. Since the number of transistors per unit area in an SRAM is as large or larger than that of any other type of digital IC, the SRAM is frequently used as a vehicle for development of new IC technologies.

For this LDRD project, we decided to evaluate the use of a Sandia developed SRAM for detecting non-corrosion temperature and humidity induced IC failures. Non-corrosion related temperature and humidity induced bit failures in SRAMs were first reported by Guan et. al[8]. According to Shirley and Hong[9], these functional failures are related to the presence of passivation defects. Examples of such defects have been given by Danielson, Marcyk, Babb, and Kudva[10].

The Sandia MDL was in the process of developing a three level metal 0.5 μm CMOS technology and as part of that development process, was building a single level metal 16K SRAM, the TA780. Since the design of the memory was available, we felt that this would be a better choice than a commercial SRAM for determining precise causes of failure after HAST exposure.

For our experiment we packaged three groups of TA780 die in ceramic DIPs. The first group of parts had had lids sealed onto the packages in a normal CHP assembly process. The second group was encapsulated in liquid epoxy, Dexter FP4450. The third group was left open and not encapsulated. All parts were electrically tested and then a HAST environmental test was started at 140°C, 85% RH and 3.3 V bias. Initial measurements were made after 10 and 20 hours exposure and unusually large numbers of failed parts were detected in both the unencapsulated and the encapsulated groups. The hermetic control parts did not show any failures.

A detailed Failure Analysis (FA) was conducted by Dept. 1275 and the final report from this study by J. M. Soden, A. N. Campbell, and D. H. Cooper is contained in Appendix A. These investigators determined that the failures were associated with a Ti deposition problem during wafer fabrication. This problem had been observed earlier but not associated at the time with humidity[11]. The consequence of this problem was a moisture activated contact resistance instability. In earlier investigations it had been determined that if the Ti layer at the bottom of a contact window was too thin, the contact resistance would eventually become high. The parts were passivated with a phosphosilicate glass (P-glass) instead of the more conventional SiN. As a result, many paths existed for moisture penetration to the die surface. This contact resistance problem was associated with two wafer lots fabricated in late 1995. The die for our experiment were taken from these lots.

Although we did not succeed in detecting the type of moisture induced failure which we had set out to find, we did demonstrate the utility of the SRAM structure for detecting moisture induced circuit failures. It is likely that a conformal and relatively defect free SiN chip passivation would have significantly decreased the failure rate which we measured. The optimum size for a test chip

memory would have to be determined in HAST experiments with SRAMs which demonstrated more usual failure rates than those which we measured.

V. Recommendation for New ATCs

A. General discussion

There traditionally have been two approaches to the use of ATCs for packaging related studies. By far the most predominate strategy has been to use chip designs intended for examination of only a few related failure modes. An example of this type of chip is our ATC02.5 which is intended only for examine of THB related Al corrosion failures. The other approach is to put many types of features or damage detectors on the die and examine all failure modes simultaneously. An example of this type of chip is our ATC03 part[12]. The major limitation of a multifunction ATC is that there may not be enough features of a given type on the die to enable detection of failure modes with a very low rate. As a result of the work performed on this LDRD project, we are in a position to recommend development of a multifunction ATC which should be able to detect most or possibly all types of failures which are associated with plastic IC packaging today.

The ability to make a multifunction ATC is much enhanced by the availability of new CMOS technologies with small feature sizes. This enables placement of many more features on a die together with the use of custom control logic to interconnect various test circuits to a limited number of bond pads. When designing test chips, there is always the question of what die size to use. Large complex die such as microprocessors typically have an edge dimension $\gtrsim$ 0.5 in. while many small die have edge dimensions in the range 0.1-0.3 in. With a 0.5 in. die it is very feasible to make a multifunction die with adequate numbers of features. We shall discuss the conceptual design for such a die.

B. Features for a new ATC

Based on the work done over the past two years we feel that the following types of circuits would be desirable on a new CMOS ATC:

1. Stress sensing cells

Mechanical stress measurement will remain a central goal in defining plastic IC reliability. There will always be a need to examine both built in stresses and the stress shifts which occur during environmental stressing or mechanical flexure of circuit boards. As a result of our work with ATC04 we feel that the basic stress sensor cell design and addressing/measurement strategy is good but that some refinements need to be made to enable measurement of in-situ thermal stresses during a temperature excursions.

The basic stress sensor cell addressing and measurement scheme which we developed during this LDRD program appear to be quite sound. It is desirable to obtain stress data along the chip diagonals and on paths along the chip edges. Typically, the in-plane compressive stress peaks in magnitude at the die center, while the shearing stress peaks in magnitude at die corners. For a future test chip, we would place stress sensor cells as close as possible to each die corner to optimize the shearing stress measurement. It may

also be possible to place a cell directly under a bondpad to detect bond related stress changes.

2. Corrosion triple track structures

The corrosion triple track structures which we used in this program appear well suited for detecting both Al conductor corrosion and also defects in chip passivation. The number of triple tracks which can be placed on a chip depends on the available space for top level metal structures. In the case of passivated structures, it appears reasonable to use the ATC02.5 and ATC02.6 schemes in which one end of each track is connected to a common bus. In this way, the number of bondpads required is minimized. For unpassivated triple tracks, there is a potential for track-to-track shorting by either particle produced conductor damage (smearing) or by conducting contaminant films. This necessitates that these structures either not be connected to a bus or that isolation be provided through CMOS transmission gates, similar to the scheme used to isolate the resistors on the ATC04 chip. The four triple tracks on ATC03 were all designed as separately bonded circuits and so they do not experience the problems which we encountered with the ATC02.6 common bus geometry.

Since unpassivated track structures are extremely sensitive to both mechanical damage and the presence of contaminants, it appears useful to employ them in a general purpose test chip. Failure of one of these structures in high voltage or environmental stressing would indicate a potential for future IC failure. However, more research is required to quantitatively define the relation between the unpassivated track failure rate and actual device failure rates.

3. Bondpad resistance test structures

The ATC02.6 bondpad transverse resistance test structure worked well in our tests and could be used in future programs without major modification. The increase in resistance with aging time correlated reasonably well with decreases in bond pull and shear strength. The spread in resistance shift values from pad to pad and from part to part was relatively small relative to the average resistance shift after environmental stressing. As a result of this observation, we conclude that a small number of pad resistance structures per die would be adequate for monitoring bond degradation during high temperature storage experiments. We suggest about five test sites per die for this function, or about 25 pads total.

4. Digital logic circuitry

Our work with the Sandia CMOS-6 SRAM was not conclusive and, as a result, we were not able to specify a memory size which would be desirable for environmental testing. Nevertheless, we did demonstrate and verify that an SRAM digital circuit was excellent for detecting environmentally induced failures. We also showed that through detailed failure analysis we could pinpoint the cause(s) of the failures. A small SRAM should certainly be included on a future ATC. The 16K size of the test SRAM appears to be

adequate for the evaluation of environmental damage to digital logic. The memory is large enough to have many potential damage sites and yet small enough to be easy to test and also not consume much die real estate. More study would be required to determine an optimum memory size for a future ATC.

5. Thermal resistance test circuits.

In many cases it is desirable to be able to measure the thermal resistance of a packaged IC with a test die. This requires the ability to heat the die with power in the range 5-30 W and to measure the die surface temperature. Early thermal test chips used resistive heaters with the heater elements spread over most of the die surface to achieve a uniform top surface power density. In the case of a general purpose ATC, there is not enough room to have a heater element cover the die top surface. Fortunately, thermal analysis software can be used to predict the temperature distribution over the chip top surface. The theoretical temperature distribution can then be used to relate the temperatures at the measurement sites on the die to the average surface temperature. We feel that the ATC04 geometry with relatively small polysilicon heaters together with the diode thermometers in the stress sensor cells is very adequate for determining thermal resistance in practical situations. In addition, the heaters can be used for chip self-heating during HAST experiments, if desired, to simulate a power producing chip. We have also used resistance temperature detection circuits on the ATC02.5 chip and found that they work well also although they are not as accurate as the diode thermometers.

6. Moisture detection circuits.

Im previous programs we developed porous Si moisture detecting ATCs. These utilize a porous Si as the dielectric in a moisture sensing capacitor structure. The substrate acted as the capacitor bottom electrode while an Al grid structure on the top of the dielectric served as a permeable top electrode. A test chip, NAT01 was fabricated and used in the DLA sponsored Plastic Package Availability program[13]. It would be desirable to incorporate a porous Si capacitor in a new ATC. However, we have not studied the problems involved with fabricating an anodized porous Si capacitor on a CMOS part. Clearly, additional research would be necessary to develop a wafer fabrication process which would allow both CMOS and porous Si to be fabricated on the same wafer or die. At this time, we can only recommend the use of a CMOS ATC and a NAT01 chip together in the same package or on the same substrate.

VI. Conclusions

In the LDRD research described in this report we have shown that a number of passive and active test circuits could be combined to make a multipurpose ATC which could detect and measure a wide variety of environmental conditions and variables. Historically, ourselves and others have tended to use ATCs with only a few functions for package process development or materials degradation studies. However, for future Sandia evaluation or "qualification" of a plastic packaging technology it will be desirable from time and cost considerations to package only one type of chip for environmental stress testing. As a result, a multifunction ATC will be highly desirable for packaging evaluation.

At the present time, the focus at Sandia is shifting to prospective use of ATCs for general purpose monitoring of electronic component degradation in weapons systems during long term storage. It will be important to verify that weapons in storage have not experienced unusual excursions in temperature, humidity, or chemical environment. Although individual ICs can still fail through extrinsic or defect related processes, it will be important to verify that conditions do not exist which can or will produce general and widespread IC failures.

As we have demonstrated in this work, the circuits which we have developed and tested would be well suited for the environmental monitoring function in deployed weapons. Although in some cases, such as temperature and mechanical stress, we can directly measure the input or stress variable, in other cases such as corrosion of triple tracks or SRAM bit errors, we detect the consequences of the presence of damaging environmental conditions.

On the basis of the work which we have done on the *High-Reliability Plastic Packaging for Microelectronics* LDRD, we feel that continued development of multifunction ATCs would be highly desirable and valuable for future Defense Programs. The next logical step in such a development program would be to demonstrate through experimentation on a model weapons electronics system that a multifunction ATC could, in fact, detect the presence of potentially damaging environments before actual ICs started to fail.

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VIII. Appendix A. Memo on SRAM Failure Analysis

Sandia National Laboratories

Operated for the U.S. Department of Energy by

Sandia Corporation

Albuquerque, New Mexico 87185-1081

date: October 7, 1996

to: James N. Sweet, MS-1082 (D/1333)

from: Jerry M. Soden, Ann N. Campbell, and Dan H. Cooper, MS-1081 (D/1275)

subject: Plastic Package LDRD Failure Analysis Interim Report

Background

In May, 1996, Dept. 1275 was requested to assist with failure analysis, evaluation of preliminary test data, and experiment planning for this project. During the first meeting on 5/21/96, the status of the project was reviewed (attendees: Ann Campbell, Rich Flores, Robert Mitchell, Dave Peterson, Jerry Soden, and Jim Sweet). Three groups of TA780 16K SRAMs had been packaged early in 1996 in ceramic 24 pin DIPs as follows: (1) Control: 14 ICs packaged using the normal hermetic process; (2) Bare: 15 ICs packaged normally, except lids were not installed; and (3) Glob: 30 ICs packaged normally, except an epoxy (Dexter 4450) coating was used to cover the die and no lids were installed. The epoxy was used to simulate a plastic package. During the time period from January to late April, all three groups of ICs had been electrically tested prior to HAST (Highly Accelerated Stress Test) and then exposed to a total of 20 hours of HAST (140 °C, 85% RH, 3.3 V static bias). Electrical testing was performed using the Advantest T3342. An interim test was performed at 10 hours. After both the 10 hour and 20 hour HAST, an unexpectedly high number of bare and glob ICs failed the electrical tests, while the controls behaved as expected (some ICs in all groups failed several continuity and read timing tests due to known test fixture and program conditions).

Analysis Summary

Preliminary review of the electrical test data indicated that randomly occurring bit errors were responsible for the IC failures. Several quick experiments were performed to investigate the

repeatability and dependencies of the bit failures. The experiments included retests first at 3.3 V, then 4.5 V, followed by 3.3 V to evaluate the effects of elevated voltage and to assess the repeatability of the failure mode. A vacuum bake was performed to evaluate whether unbiased ICs would recoverer in a hot, dry environment (110 °C, 0.2 Torr). The data for these experiments were analyzed and compared to the post-HAST data. Initial review of these data showed that some changes occurred in the location of failing bits but many of the bits failed repeatedly.

A more thorough analysis was performed by manually comparing failing data patterns for three of the Advantest data files. Two of these data files (prfla_fn.asc and prfb_map.asc) were created pre-vacuum bake testing and the other file (pflc_map.asc) was created during post-vacuum bake testing. The data in these files were compared in two ways. First, failing data patterns were compared in the two pre-bake data files (prfla_fn.asc and prfb_map.asc). Significant differences in the location of the failing bits were found for the following ICs: G262, B277, B280, and B285. Then, failing data patterns in one of the data files generated before the bake (prfb_map.asc) were compared with the data file generated after the bake (pflc_map.asc). Significant differences in the location of the failing bits were found for the following ICs: G260, G261, G262, G263, G266, G271, G273, G299, G302, B274, B275, B276, B277, B278, B280, B285 and B286.

The bare and glob ICs failed for all three types of data patterns used for the electrical tests: the Unique Address pattern, Checkerboard pattern, and Complement Checkerboard pattern. Two types of failure modes, bits stuck high and bits stuck low, were observed to occur in an apparently random manner. It was also observed that there appeared to be a significant occurrence of bits failing in pairs of physically adjacent memory cells.

The failures of bit pairs had been investigated earlier this year by Alan Liang (1275) and others. The result of their investigation was the conclusion that the root cause was high resistance contacts. It was found that if the Ti layer deposited at the bottom of the contact windows is too thin, the contact resistance is high [1,2]. In the TA780 layout, adjacent cells share a common contact which, if its resistance is above about 200 Ω, can cause both cells to experience a read disturb (change of data during the read operation). Fig. 1 shows the layout for the SRAM cell and indicates the V_{SS} contacts on each side of the cell that are shared with the adjacent cells. Fig. 2 shows the schematic for two cells and the shared V_{SS} contact. Figs. 3 and 4 show simulated waveforms for a normal read and a read disturb. The Ti layer thinning appears to have occurred randomly in the two wafer lots (BL04720 and BL04722A) used for this LDRD project. Both of these lots were fabricated during the late 1995 time period when the first wafer lots with the contact resistance problem were made.

To evaluate the effect of HAST on contact resistance, contact string test structures from the HAST project wafers were packaged in a bare die condition. The metal-1 to *n*+ strings were evaluated (a masking problem made the *p*+ strings unusable). The resistance of these structures was tested before and after a short HAST exposure (20 hour, 140 °C, 85% RH, unbiased). It was found that the resistance changed significantly, with increases ranging from 12% to 70%.

As a result of this work, it was concluded that the high failure rate for the ICs in the HAST experiment was caused by a moisture activated, contact resistance instability related to the Ti

deposition problem. Focused ion beam (FIB) cross sections of suspect contacts were made but, like those obtained by Alan during his earlier investigation, no microstructural anomalies were observed (supporting the conclusion that this failure mechanism involves the W/Ti/Si interface when the Ti is thin). FIB passive voltage contrast images and optical inspection found evidence of a rough or textured "corrosion" feature in the passivation next to the bond pad openings and at sites in the memory array, some of which appeared to correlate with contacts (Figs. 5 and 6).

During meetings in August, it was decided to consider abandoning the work on the first group of ICs and starting a new packaging group. Because of the contact resistance problem and also the I_{DDQ} testability limitations of the TA780s (due to their self-timed design), the possibility of using TA786s for the new group was considered. The TA786s are a static (not self-timed) version of the TA780 and therefore have high I_{DDQ} testability (a very desirable feature for the investigation of the type of transistor instabilities anticipated during HAST). This was discussed with Rich Flores. Rich had a group of TA786 die from a recent lot with good yield (BD08903A). Rich felt these would be a good choice, but he indicated there is a design issue with these ICs to be considered. In converting to the static design, the circuitry for four inputs (PC, WL, SNS, and LATCH) were inadvertently left with one input of a 2-NOR unconnected. Although this input is logically unused, the result is a floating input that can cause high I_{DDQ} for certain logic states. Since this would detract from the ability to detect HAST-induced parametric effects with thorough I_{DDQ} testing, methods for connecting the input to V_{SS} (the noncontrolling state) were considered.

It was decided to send four die to a focused ion beam service company (Beam-It, Inc.) for circuit modifications to connect these inputs to V_{SS}. At this company, a platinum deposition was used that may be more robust in a HAST environment than tungsten (the other commonly used FIB deposition material and the metal presently being used in Dept. 1275's Micrion FIB system). These die have been packaged and are waiting for an Advantest I_{DDQ} test program to be created.

If these ICs perform as expected during I_{DDQ} testing and a short HAST experiment, a decision will be made whether to modify an additional 40 to 50 TA786s or wait for a new wafer lot (a layout fix has been implemented that eliminates the floating input circuity). The cost of modifying 40-50 die is estimated to be between $10K and $15K. The Advantest I_{DDQ} test program is expected to be available the first part of October.

Memo References

1. A.Y. Liang. P. Tangyunyong, R.S. Bennett, R.S. Flores, J.M. Soden. and E.I. Cole, "Failure Analysis of a Half-Micron CMOS IC Technology," Int. Symp. for Testing and Failure Analysis, Nov. 1996.

2. J.M. Soden, R.E. Anderson, and C.L. Henderson, "IC Failure Analysis Tools and Techniques - Magic, Mystery, and Science," Int. Test Conf., Lecture Series 2, Oct. 1996.

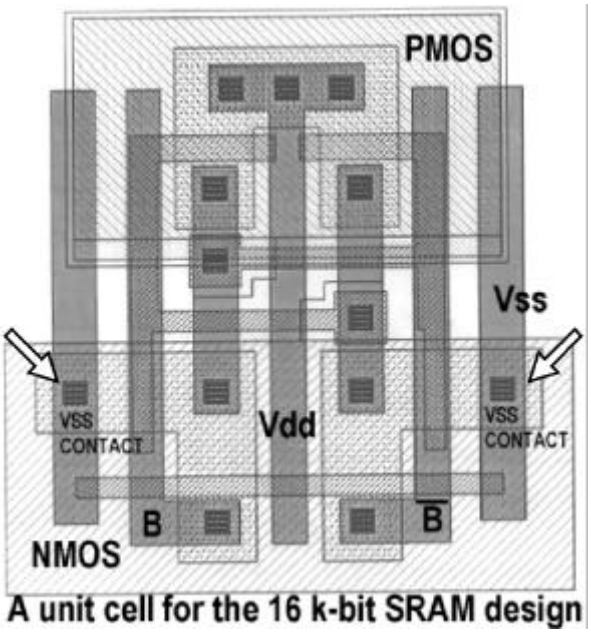

Fig. 1. Layout for a unit cell for the SRAM. The shared V_{SS} contacts are indicated by arrows.

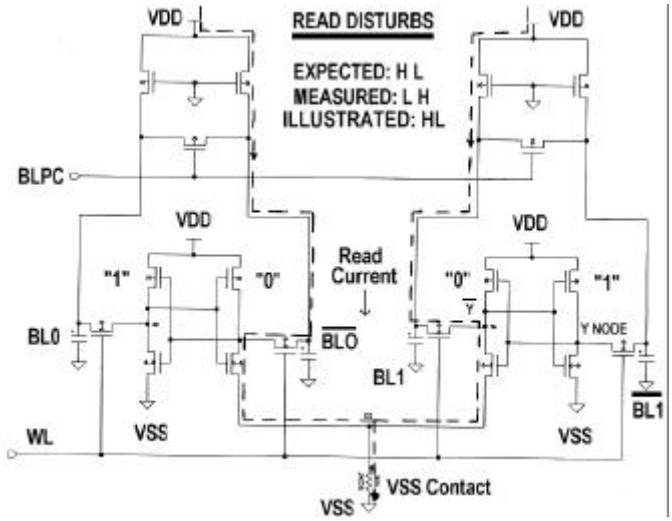

Fig. 2. Schematic for two adjacent SRAM cells. Note the shared V_{SS} contacts at the bottom.

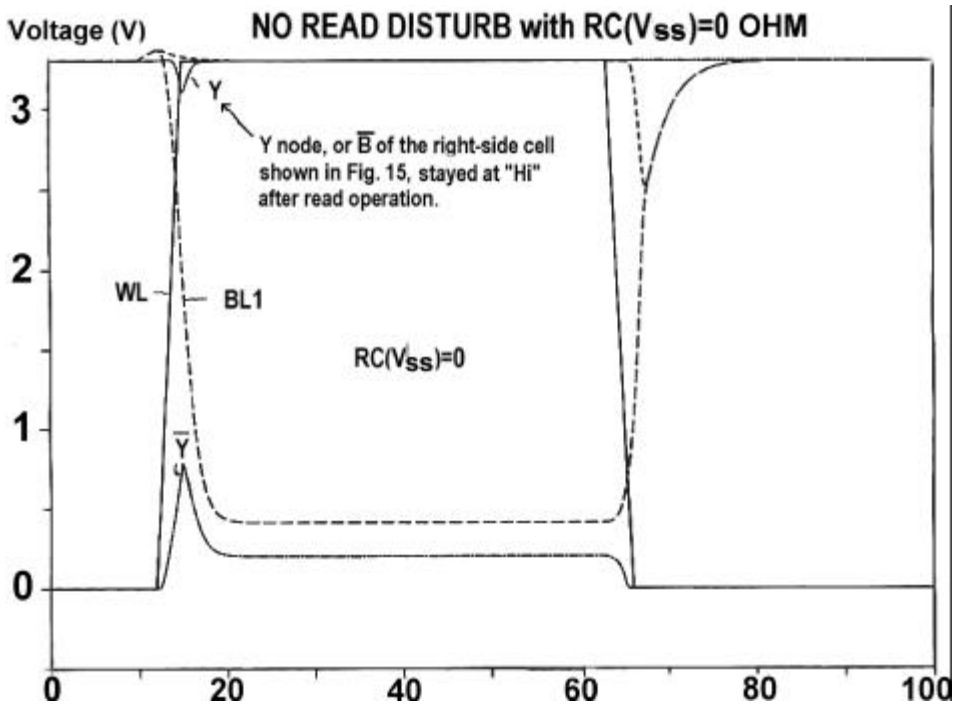

Fig 3. SPICE simulation timing diagram showing a normal read operation with R_C = 0 Ω (refer to the schematic in Fig. 2).

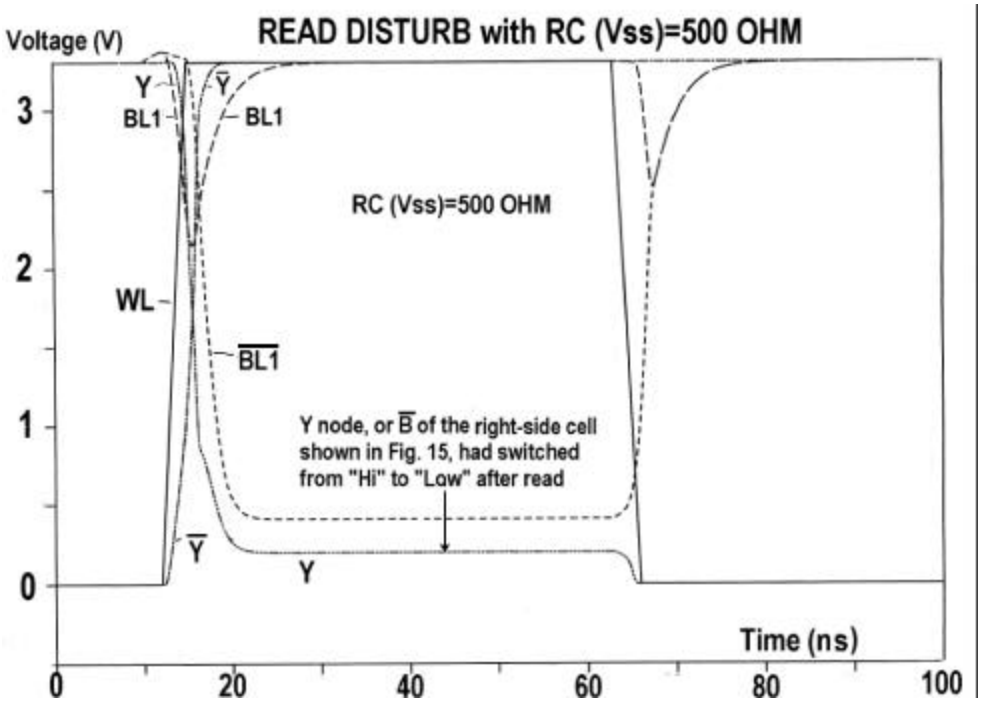

Fig. 4. SPICE simulation timing diagram showing a read disturb operation with R_C = 500 Ω (refer to the schematic in Fig. 2).

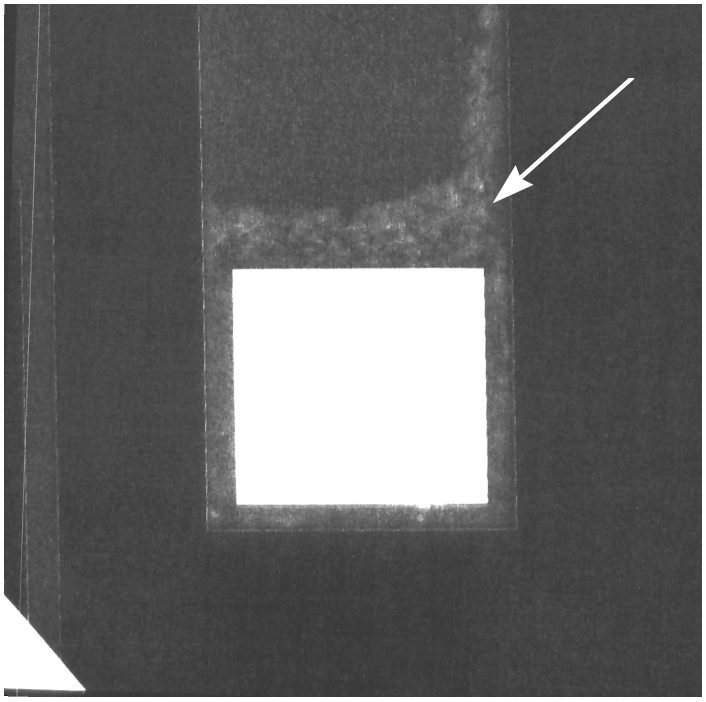

Fig. 5. FIB voltage contrast image of “corrosion” in bond pad region.

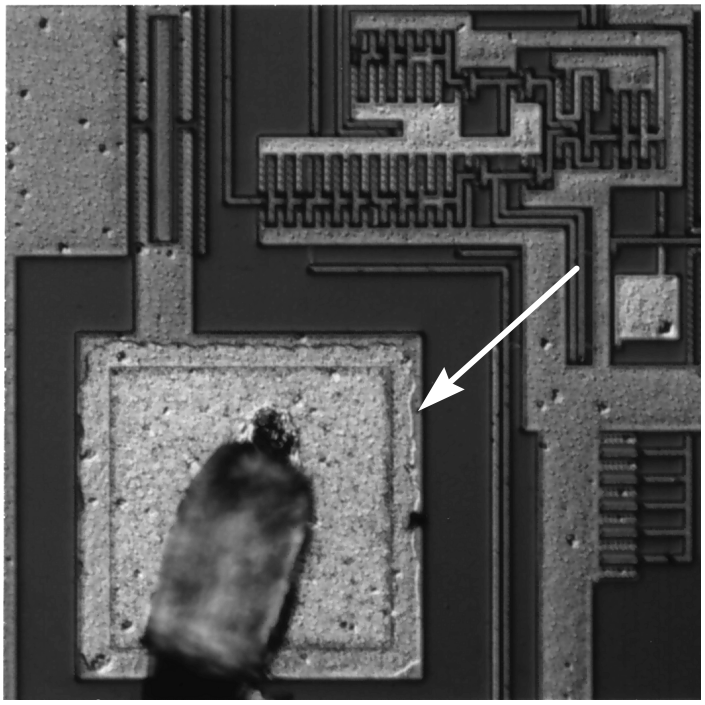

Fig. 6. Optical image of “corrosion” in bond pad region.

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